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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,738	10/01/2004	Jen-Ying Chen	FTCP0043USA	5737

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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
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EXAMINER	
DILLON, SAMUEL A	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
08/24/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/711,738	CHEN, JEN-YING	
	Examiner	Art Unit	
	Sam Dillon	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8,10 and 11* is/are rejected.

7)☒ Claim(s) *2-7 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/1/04* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Examiner acknowledges the applicant's submission of the amendment dated May 24, 2007. Per the amendment, Claims 1, 8 and 10 have been amended and Claim 11 has been added. The instant application having Application No. 10/711,738 has a total of 11 claims pending in the application; there are 3 independent claims and 8 dependent claims, all of which are ready for examination by the examiner.

I. RESPONSE TO AMENDMENT(S) / ARGUMENT(S)

2. Applicant's arguments with respect to the 35 U.S.C. 102(b) rejections of Claims 1, 8 and 10 have been fully considered but they are **not persuasive**.

3. Regarding Claim 1, the Applicant contends that the claims require and Cucchi does not teach that the write blocking logic comprises a write select counter or a read select counter that count how many data the configurable write buffer has ever stored or transferred. The Examiner respectfully disagrees with this requirement, and notes that the claimed limitations read *"a write select counter for ..."* and *"a read select counter for ..."*. These limitations are interpreted as claiming intended use. The Applicant is directed to Section II of this action for more information. Accordingly, Cucchi discloses a write counter and a read counter *(column 2 lines 36-45)* that are inherently capable of representing a number, and are then not precluded from the intended use.

4. Regarding Claim 1, the Applicant contends that the claims require and Cucchi does not teach a *"demultiplexer for ..."* and a *"multiplexer for"*. The Examiner respectfully disagrees, and notes that the claimed limitations are interpreted as claiming intended use. The Applicant is directed to Section II of this action for more information. Accordingly, Cucchi discloses a multiplexer *(column 1 lines 50-53)* that is not precluded from the intended use, and additionally

the single port RAM can be considered a demultiplexer, in that it takes one data input and a number of selection inputs, and can have several outputs *(column 1 lines 50-53)*.

5. Regarding all other Claims not specifically traversed above and whose rejections were upheld, the Applicant contends that the listed claims are allowable by virtue of their dependence on other allowable claims. As this dependence is the sole rationale put forth for the allowability of said dependent claims, the Applicant is directed to the Examiner's remarks above. Additionally, any other arguments the Applicant made that were not specifically addressed in this Office Action appeared to directly rely on an argument presented elsewhere in the Applicant's response that was traversed, rendered moot or found persuasive above.

II. OBJECTIONS TO THE APPLICATION

6. Claims 1, 2, 8, 9, 10 and 11 are objected to because of the following informalities:

a. Claims 1, 8 and 10 read *"the single port memory unit **for**", "a configurable write buffer ... **for** ... and **for**", "a write blocking logic ... **for** ... and **for**", "a write select counter **for**", "a read select counter **for**", "a demultiplexer **for**", "a multiplexer **for**"* and *"an arbiter ... **for**"*. These limitations are interpreted as claiming intended use.

A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See MPEP 2106 II (C).

b. Claims 2, 9 and 11 read *"a first counter **for**", "a write comparator ... **for**", "a read comparator .. **for**", "wherein the write select counter is ... **for**", "and the read select counter is ... **for**", "a plurality of buffer modules **for**", "wherein the demultiplexer is ...*

for", and *"the multiplexer is ... **for***". These limitations are interpreted as claiming intended use.

Appropriate correction is required.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102 - Cucchi

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claims 1, 8 and 10** are rejected under 35 U.S.C. 102(b) as being anticipated by Cucchi et al. *(US Patent Number 4,899,352)*.

9. As per **Claim 1**, Cucchi disclose(s) a synchronous memory device with a single port memory unit, the synchronous memory device comprising:

the single port memory unit *(RAM 10, figure 3)* for storing data according to a predetermined clock *(ck channel, figure 3)*;

a configurable write buffer electrically *(FIFO, figure 3)* connected to the single port memory unit for storing data according to the predetermined clock and for transferring its stored data to the single port memory unit according to the predetermined clock *(LFIFO is a dependency of the RAM access control logic, which is a dependency of ck channel, figure 3)*;

a write blocking logic *(write and read counts 14 and 16, figure 3)* electrically connected to the configurable write buffer for estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to

store data according to the predetermined clock, and for controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal *(signal from RAM access control logic 18 to write count 14, figure 3)*; wherein the write blocking logic comprises:

a write select counter *(write counter, column 2 lines 36-45)* for counting how many data the configurable write buffer has ever stored;

a read select counter *(read counter, column 2 lines 36-45)* for counting how many data the configurable write buffer has ever transferred;

the configurable write buffer comprises:

a demultiplexer *(single port RAM, column 1 lines 50-53)* for storing data to the configurable write buffer according to the write select counter; and

a multiplexer *(MUX, column 1 lines 50-53)* for transferring data to the configurable write buffer according to the read select counter; and

an arbiter *(RAM access control logic 18, figure 3)* electrically connected to the write blocking logic and the single port memory unit for generating the write acknowledge signal.

10. As per **Claim 8**, Cucchi disclose(s) a synchronous\asynchronous memory device with a single port memory unit, the synchronous\asynchronous memory device comprising:

the single port memory unit *(RAM 10, figure 3)* for storing data according to a read clock *(ck channel, figure 3)*;

a configurable write buffer *(FIFO 28, figure 3)* electrically connected to the single port memory unit for storing data according to a write clock *(ck source, figure 3)* and for transferring its stored data to the single port memory unit according to the read clock;

a write blocking logic *(write and read counts 14 and 16, figure 3)* electrically connected to the configurable write buffer for estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to store data according to the write clock *(data is recorded in according to the ck source clock signal, so can be construed as being a dependency of the loading of the FIFO, figure 3)*, and for controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal (*signal from RAM access control logic 18 to write count 14, figure 3)*; wherein the write blocking logic comprises:

a write select counter *(write counter, column 2 lines 36-45)* for counting how many data the configurable write buffer has ever stored;

a read select counter *(read counter, column 2 lines 36-45)* for counting how many data the configurable write buffer has ever transferred;

the configurable write buffer comprises:

a demultiplexer *(single port RAM, column 1 lines 50-53)* for storing data to the configurable write buffer according to the write select counter; and

a multiplexer *(MUX, column 1 lines 50-53)* for transferring data to the configurable write buffer according to the read select counter; and

an arbiter *(RAM access control logic 18, figure 3)* electrically connected to the write blocking logic and the single port memory unit for generating the write acknowledge signal.

11. As per **Claim 10**, Cucchi disclose(s) a computer system comprising:

a first computer operating on a first clock *(source of 'data in', figure 3)*;

a second computer operating on a second clock different from the first clock *(receiver of 'data out', figure 3)*; and

a memory device *(figure 3)* comprising:

a single port memory unit *(RAM 10, figure 3)* for storing data according to the first clock *(data is loaded into the memory device according to ck source initially, figure 3)*;

a configurable write buffer *(FIFO 28, figure 3)* electrically connected to the single port memory unit for storing data transferred from the first computer according to the first clock *(data is recorded in according to the ck source clock signal, so can be construed as being a dependency of the loading of the FIFO, figure 3)* and for transferring its stored data to the single port memory unit according to the second clock *(LFIFO is a dependency of the RAM access control logic, which is a dependency of ck channel, figure 3)*;

a write blocking logic *(write and read count's 14 and 16, figure 3)* electrically connected to the configurable write buffer for estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to store data transferred from the first computer according to the first clock *(all data is transferred from the first computer according to the first clock, figure 3)*, and for controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal *(signal from RAM access control logic 18 to write count 14, figure 3)*; wherein the write blocking logic comprises:

a write select counter *(write counter, column 2 lines 36-45)* for counting how many data the configurable write buffer has ever stored;

a read select counter *(read counter, column 2 lines 36-45)* for counting how many data the configurable write buffer has ever transferred;

the configurable write buffer comprises:

a demultiplexer *(single port RAM, column 1 lines 50-53)* for storing data to the configurable write buffer according to the write select counter; and

a multiplexer *(MUX, column 1 lines 50-53)* for transferring data to the configurable write buffer according to the read select counter; and

an arbiter *(RAM access control logic 18, figure 3)* electrically connected to the write blocking logic and the single port memory unit for generating the write acknowledge signal.

12. As per **Claim 11**, Cucchi disclose(s) the computer system of Claim 10, wherein the configurable write buffer further comprises:

a plurality of buffer modules *(innards of the single port RAM, column 1 lines 50-58)* for storing data;

wherein the demultiplexer is electrically connected to the buffer modules for storing data to one of the buffer modules according to the write select counter *(as the demultiplexer was interpreted as the single port RAM, it can be said to be electrically connected to it's own insides, column 1 lines 50-58)*; and

the multiplexer is electrically connected to the buffer modules for transferring data stored in one of the buffer modules to the single port memory unit according to the read select counter *(figure 2)*.

IV. CLOSING COMMENTS

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

a. STATUS OF CLAIMS IN THE APPLICATION

13. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(1). SUBJECT MATTER CONSIDERED ALLOWABLE

14. Claim 2-7 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

a(2). CLAIMS REJECTED IN THE APPLICATION

15. Per the instant office action, Claims 1, 8, 10 and 11 have received an action on the merits and are subject of a final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 9:30-6:00.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

IMPORTANT NOTE

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SAD

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Art Unit 2185

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